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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)	
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		<u>10/603,640</u>	<u>6/25/03</u>
		First Named Inventor	
		<u>Marcus May</u>	
Art Unit	Examiner		
<u>2857</u>	<u>Gutierrez, Anthony</u>		
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>33,534</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 <u></u></p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below".</p> <p><input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.</p>			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Marcus May

Serial No: 10/603,640

Filing Date: 6/25/03

Title: METHOD AND APPARATUS FOR EFFICIENT BATTERY USE BY A
HANDHELD MULTIPLE FUNCTION DEVICE

Examiner: Guterrez, Anthony

Art Group: 2857

Docket No: SIG000085

Date: 2/17/06

Pre-Appeal Brief Request for Review

1. In the Final Office Action dated August 23, 2005, the Examiner reasserted the rejection of claims 1, 5-7, 8, 11, 12, 14-16, 20-23, 26, 27, 29, and 30 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669); claims 2, 9, 17, and 24 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) and in further view of Barker (U.S. Patent No. 3,609,504); and claims 3, 4, 10, 13, 18, 19, 25 and 28 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) in further view of Patel (U.S. Patent No. 5,018,148). In addition, the Examiner stated in the Final Office Action that the applicant's arguments of 6/15/05 are not persuasive and points to column 4, lines 30-34, column 4, line 64, through column 5, line 19, and column 8, line 58, through column 9, line 25 of Choudhury as teaching the features of the present invention.

2. Claims 1, 5-7, 8, 11, 12, 14-16, 20-23, 26, 27, 29, and 30 have been rejected under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669).

In particular, Urbano does not teach efficient use of a battery in a handheld device to initiate one of a plurality of fail safe algorithms based on when one or more of the

overload condition, the system low voltage condition, and the battery low voltage condition are detected. Urbano, however, does teach an ultrasound system that includes techniques to reduce power consumption. For instance, Urbano teaches that power consumption by electrical components is reduced in one or both of the ultrasound data path and the ultrasound processing control. (column 3, lines 12 – 15 and column 5, lines 1 – 9).

Urbano further teaches that, during the non-use periods, the low power mode or decreased power state may be achieved in a variety of ways. For example, Urbano discloses at column 5, lines 47 – 50, a reduced clock rate; at column 5, lines 62 – 66, a standby mode or suspend mode; at column 6, lines 5 – 21, a return to initialization state; and at column 6, lines 28 – 31, a reduced power supply state.

Urbano further teaches that the various lower power states may be initiated in a variety of ways. For example, Urbano discloses that a user activated button (column 7, lines 4 – 6), expiration of an inactivity time out period (column 7, lines 14 – 17), expiration of a wait to receive input time period (column 7, lines 20 – 22), and a user configuration (column 7, lines 33 – 36).

Accordingly, Urbano teaches an ultrasound system that has power reduction techniques to place un-used components into low power states that may be initiated in a variety of ways. Urbano does not teach or suggest sensing for one or more of low battery, overload, or system low voltage and initiating a fail safe algorithm in response thereto.

Choudhury teaches a digital signal processor controlled uninterruptible power supply (UPS), where the basic architecture of the UPS is shown in Figure 2 and the DSP of Figure 3 produces the pulse width modulated (PWM) control signals for transistors 211, 213, 241, 251, 231, and 233 of Figure 2. The UPS has two modes of operation: a normal mode and a battery back up mode. In the normal mode, the UPS produces an AC output and charges the battery. In the battery back up mode, the UPS converts the battery

voltage to a DC bus voltage and, via a DC-AC inverter, produces the AC output from the DC bus voltage. (column 3, lines 28 – 44)

Choudhury teaches that the DSP produces the PWM control signals PWM1 – PWM6 (column 4, lines 45 – 49) by performing the functions of Figures 5 – 13. In Figure 10 and the corresponding text at column 8, lines 22 – 57, the DSP produces PWM5 and PWM6 signals for transistors 231 and 233 such that the DC/AC inverter portion of the UPS is regulated. The PWM5 and PWM6 signals are produced by comparing a digitized output voltage (V_{out}) with a reference sinusoid waveform (V_{ref}) to produce a difference. The difference is processed by a compensator (P11) to produce a reference current for an inner current loop. In addition, a digitized inductor current feedback (I_{out}) is compared with the output of the first compensator (P11) to produce a second difference. A second compensator (P12) produces PWM5 and PWM6 signals from the second difference.

In Figure 11 and the corresponding text of column 8, line 58, through column 9, line 25, Choudhury teaches that the DSP generates a PWM3 signal and disable a PWM4 signal for charging the 110 volt DC battery 105 from the 400 volt DC bus. In this mode, the DSP senses the battery current (I_b), the battery voltage (V_b), and V_- with respect to ground. The battery voltage and battery current are used to determine which of the three battery charge modes (e.g., trickle, bulk charge, and over charge) to initiate.

In Figure 12 and the corresponding text of column 9, line 26, through column 10, line 11, Choudhury teaches that the DSP generates PWM1 and PWM2 signals to regulate the DC bus to 400 volts DC. To do this, the DSP senses the AC input voltage (V_s), the AC input current (I_s), and the DC bus voltage (V_- , V_+). Based on these inputs, the pulse width of PWM1 and PWM2 signals is determined such that the DC bus is regulated to 400 volts.

In Figure 13 and the corresponding text of column 10, lines 12 – 35, Choudhury teaches that the DSP generates PWM4 signal and disables PWM3 signal to produce a boost converter for the battery back up mode. In this mode, the DSP senses the battery

current (Ib), the battery voltage (Vb), and V- with respect to ground to establish the pulse width of the PWM4 signal.

From the above passages, Choudhury teaches a UPS that has a DSP producing the control signals for the normal mode and the battery back up mode of the UPS. Choudhury does not teach or suggest sensing for one or more of low battery, overload, or system low voltage and initiating a fail safe algorithm in response thereto.

Since each of the independent claims 1, 8, 12, 16, 23, and 27 of the present patent application includes a limitation for sensing a low battery condition, an overload condition, or a system low voltage condition and initiating a fail safe algorithm in response thereto, the applicant believes that the combination of Urbano with Choudhury fails to render the present claims obvious. In particular, the power reduction techniques of Urbano in combination with the normal and battery back up modes of generating PWM signals of Choudhury do not suggest a method and apparatus for initiating a fail safe algorithm in response to sensing a low battery condition, an overload condition, and/or a low system supply voltage condition.

3. Claims 2, 9, 17, and 24 have been rejected under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) and in further view of Barker (U.S. Patent No. 3,609,504).

As demonstrated above, the combination of Urbano and Choudhury fail to render the independent claims of the present patent application obvious. Thus, the applicant believes that the present claims are not obvious in view of the cited prior art.

4. claims 3, 4, 10, 13, 18, 19, 25 and 28 under 35 USC § 103 (a) as being unpatentable over Urbano (U.S. Patent No. 6,592,521) in view of Choudhury (U.S. Patent No. 6,169,669) in further view of Patel (U.S. Patent No. 5,018,148).

As demonstrated above, the combination of Urbano and Choudhury fail to render the independent claims of the present patent application obvious. Thus, the applicant believes that the present claims are not obvious in view of the cited prior art.

RESPECTFULLY SUBMITTED,

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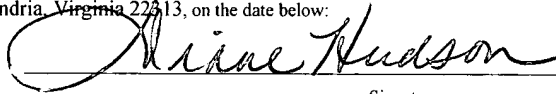
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37 C.F.R. 1.8

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Date



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